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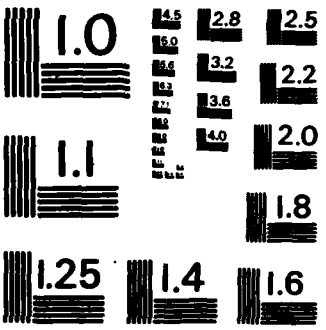

Functional Testing of LSI/VLSI Based Systems with Measure of Fault Coverages

SCIENTIFIC AND TECHNICAL REPORT

FIRST QUARTERLY STATUS REPORT

Prepared By

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A. Contractor's name and address:

The Research Foundation of
State University of New York
P.O. Box 9
Albany, NY, 12201

B. Contract No. DAAB07-82-K-J056

C. Date of Report: August 6, 1982

D. Title: Tne First Quarterly Report

E. Period Covered: April 28 to July 28, 1982

F.-H. Description of Progress:

We started the project by initiating a study of available literature that is related to the scope of work for this project. Testing of high complexity LSI and VLSI components has become very important, and has been receiving considerable interest.

The project involves a test-effectiveness measure. Because of the complexity of the problem, it has not yet been satisfactorily approached by others. Some work on information theoretic approach has been reported [1], but the approach does not appear to be suitable for testing digital system with high fault coverage. We feel that test-effectiveness measure should be related with physically possible failures, and thus the measure should be able to use detailed information of the circuitry if it is available.

The fault-classes approacn (equivalent functional faults), as suggested in the proposal for this project, appears promising, and is being investigated.

For logic with known overall function but unknown implementation, a coverage measure may be found by considering the number of random vectors applied. Some data is available, which correlates coverage (in terms of stuck-at-faults) with number of vectors applied. It has been noticed that coverage versus number of vectors curves are different for regular structures like PLA (Programmable Logic Array) when compared with random logic. This suggests that regularity of implementation should be considered an important parameter in random testing, or else analysis of regular structures should be considered separately.

We have looked at the papers published in the most recent Proceedings of the 12th International Symposium on Fault-Tolerant Computing and found that references No. 2 and 3 to be closest related to this project.

Reference No. 2 suggests an interesting design for micro-processors which makes them very testable. An important part of this paper is devoted to the microprogram control. It proposes a two-level design of control unit. One level generates only labels for microinstructions, which themselves are fetched from another storage.

The system uses the following four modes:

Mode 0: Normal

Mode 1: all registers in CPU including the flags can be read or written from outside.

Mode 2: micro-instructions can come from outside.

Mode 3: normal execution and label available on the address bus. Label and address share a common bus.

Only two extra pins are needed for distinguishing among the above four modes of operations.

In the proposed design, both label-sequence for a specific instruction, and execution of specific microinstructions can be separately tested.

Our project deals with commercially available components instead of designing new microprocessors for testability. But, Reference No. 2 does point out the difficulty of testing the control unit. We will have to develop a method which can, hopefully, accomplish close to what the design in [2] allows in a straightforward way.

In [3], an approach to test "errors" rather than "faults" is presented. The concept of 'structured testing' as borrowed from software testing is used. The approach attempts to test all micro-operations, such that a micro-operation is tested by executing an instruction sequence, in which all other micro-operations have been previously tested. This approach does not seem to be applicable to our project as it does not consider physical faults. However, structured testing has some advantages if one is interested in fault location. It has limited advantage if only detection is of interest.

From examination of current literature, it is apparent that testing of control units and interrupt/DMA capabilities are relatively unsolved problems. We are considering fault models for these. For the purpose of automatic test generation, we are attempting to identify a register-transfer type of hardware description language, capable of

describing the behavior of integrated circuit chips.

Primary investigations shows a register transfer language (RTL) seems to be quite suitable for describing the behavior of components such as multiplier, calculator, instruction set of microprocessor [4]. Based on the RTL description of a digital system, a data graph can be drawn to show the relationships among RTL statements. Our goal is to use the existing path sensitizing method or D-algorithm [5] on the data graph for the purpose of detecting functional faults in the structure (data) part of a digital system. If there is a fault in control unit (e.g., a control variable has a wrong value), it becomes more complicated. However, our recent results show that there is a possibility that the similar technique may be used for faults in the control variables [6]. We plan to look further into this.

[1] V.D. Agrawal, "Information theory in digital testing", Proc. ICCC, Port Chester, New York, 1981, pp. 928-931.

[2] R. Parthasarathy, S.M. Reddy and J.G. Kuhl, "A testable design of general purpose microprocessors", Proc. 12th International Symposium on Fault-Tolerant Computing, June 1982, pp. 117-124.

[3] M.A. Annaratone and M.G. Sami, "An approach to functional testing of microprocessors", Proc. 12th International Symposium on Fault-Tolerant Computing, June 1982, pp. 158-164.

[4] S.Y.H. Su and Y.I. Hsieh, "Testing functional faults in digital systems described by register transfer language", Proc. of 1981 International Test Conference, Philadelphia, PA, Oct. 27-29, pp. 447-459.

[5] J.P. Roth, "Diagnosis of automata failures: A calculus and a method", IBM Journal of Research and Development, Vol. 10, pp. 278-291, July 1966.

[6] Y. Min and S.Y.H. Su, "Testing functional faults in VLSI", Proc. of the 19th Design Automation Conference, Las Vegas, Nevada, June 14-16, 1982, pp. 384-392.

CONTRACTOR COST CORRELATION DATA

For Quarterly Status Report

August 6, 1982

A. Budget plans: (Rough Estimate

Quarter 1:	$ 6,500	Quarter 5:	$30,000
Quarter 2:	30,000	Quarter 6:	20,000
Quarter 3:	20,000	Quarter 7:	20,000
Quarter 4:	13,500	Quarter 8:	18,808
Year 1:	$70,000	Year 2:	$88,808
(4/28/82 to 4/27/83)		(4/28/83 - 4/28/84)	

B. Current quarter actual cost: $6,530.34

C. Cumulative cost to date: $6,530.34

D. Estimate to complete as basic (predicted upon completion within contract balance).

E. Estimated monthly cost:

1982		1983		1984	
May	$ 0	January	$ 4,000	January	$ 7,000
June	700	February	4,500	February	6,000
July	5,800	March	4,500	March	6,000
August	4,000	April	4,500	April	6,808
September	13,000	May	5,000		
October	13,000	June	12,500		
November	9,000	July	12,500		
December	7,000	August	10,000		
		September	5,000		
		October	5,000		
		November	7,000		
		December	6,000		

END

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